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PATENTS
LT-5 REISSUE

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION FOR REISSUE
OF U.S. PATENT 4,823,070

Date of Issue	:	April 18, 1989
Inventor	:	Carl T. Nelson
Title	:	SWITCHING VOLTAGE REGULATOR CIRCUIT
Assignee	:	Linear Technology Corporation
Reissue Serial No.	:	683,549
Reissue Filing Date	:	April 10, 1991
Examiner	:	K. Peckman, Art Unit 2102

SUPPLEMENTAL REISSUE DECLARATION

I, CARL T. NELSON, the named inventor of United States patent 4,823,070, and the applicant for reissue thereof, declare that:

1. I am a citizen of the United States residing at 1167 Settle Avenue, San Jose, California 95125.

2. I have reviewed and understand the contents of the specification of the present reissue application, including the claims, as amended by the Response To Examiner's Action dated February 24, 1992 and the Response To Examiner's Action dated March 7, 1994, and verily believe that I am the original, first and sole inventor of the "Switching Voltage Regulator Circuit" invention described and claimed in that specification and for which a reissue patent is being sought.

3. I make this supplemental declaration under 37 C.F.R. 1.175 in support of this application for reissue.

4. Upon information and belief, United States patent 4,823,070 ("the '070 patent") is partly inoperative by reason of my having claimed, as the patentee, less than I had a right to claim, in that the claims of the patent include

limitations that were not and are not required to distinguish patentably my invention over the prior art.

5. In the first declaration that I made in support of the present reissue application (dated April 5, 1991 and entitled "REISSUE DECLARATION AND POWER OF ATTORNEY"), I identified unnecessary limitations in the claims of the patent directed to an integrated circuit having "at most" five terminals for implementing a switching voltage regulator. (see, e.g., ¶ 5 of my April 5, 1991 declaration). In this supplemental declaration I identify additional particular errors in the other claims of the patent which also unnecessarily limit the claimed invention.

6. The additional particular errors in the patent which also unnecessarily limit the claimed invention are the recitation in each of claims 2-39 and 56-74 of (1) means relating to operation of the integrated circuit in a fully isolated flyback mode (claims 2, 26, 56, 70-72 and 74), and/or (2) means responsive to control signals applied to a multi-function or second function terminal to perform a plurality of recited functions (claims 56 and 70-74). For example, these errors appear explicitly in independent claims 2, 26, 56 and 70-74 as follows:

Claim	Limitation
2	"... second means connected to the input and output terminals and to the control circuitry for accepting a second feedback signal between the input and output terminals indicative of a voltage developed across a winding of an external transformer, and for enabling the integrated circuit to operate in a fully isolated flyback mode ..."
	"... third means ... to disable one of the first and second means and to enable the other ..."
26	"... second means connected to at least one of the terminals and to the control circuitry for accepting a

	second feedback signal indicative of a voltage developed across a winding of an external transformer, and for enabling the integrated circuit to operate in a fully isolated flyback mode ..."
	".. mode select means ... to disable one of the first and second means and to enable the other ..."
56, 70-72, 74	"... means for programming the integrated circuit to operate in one of a normal feedback mode and a fully-isolated flyback mode ..."
56, 70, 71	"... means for trimming a flyback voltage developed across a winding of an external transformer when the integrated circuit operates in a fully-isolated flyback mode ..."
56,	"... second means ... for performing at least two of: ... frequency compensating ..., limiting peak current ..., variably limiting current .., and ... shutting down the integrated circuit ..."
70, 72, 73	"... second means ... for: ... frequency compensating ..., limiting peak current ..., variably limiting current .., and ... shutting down the integrated circuit ..."
71, 74	"... second means ... for: ... frequency compensating ..., limiting peak current ..., and ... variably limiting current ..."

These limitations are incorporated in claims 3-25, 27-39 and 57-69 which depend directly or indirectly from independent claims 2, 26 and 56 respectively.

7. The foregoing errors arose from inadvertence, accident or mistake, and without any deceptive intention, through my efforts during preparation and prosecution of the applications for the '070 patent to particularly point out and distinctly claim my invention based upon my understanding of the invention. In ¶ 6 of my April 5, 1991 declaration, I explained how unnecessary limitations in claims 1, 40-53 and 75-81 of the '070 patent arose during preparation and prosecution of the applications for the '070 patent by

claiming my invention in terms of circuitry to enable operation in normal feedback and isolated flyback modes and/or in terms of multiple function terminals. The unnecessary limitations of claims 2-39 and 56-74 likewise arose by claiming my invention in terms of circuitry to enable operation in normal feedback and isolated flyback modes and/or in terms of multiple function terminals.

8. The true scope of the invention disclosed in the '070 patent, as claimed in new reissue claims 86-92 (including two independent claims 86 and 89), was not fully appreciated by me at the time the applications for the '070 patent were prepared and prosecuted. My invention of a current-mode switching voltage regulator integrated circuit incorporating a power switching transistor structure, duty cycle control circuitry, error signal circuitry, comparator circuitry and a current sense resistive element, was not accomplished by any prior art. Nor did any prior art incorporate in the same integrated circuit a shutdown circuit for placing the integrated circuit into a shutdown state where the current drawn by the integrated circuit is reduced (which, as I point out below, is included in independent claim 86, but not independent claim 89).

9. The foregoing errors were discovered during or about February-March 1994, while the '070 patent was being studied by me, counsel for Linear Technology Corporation (the assignee of the '070 patent)) and Robert C. Dobkin (Vice President, Engineering, of Linear Technology Corporation), during a review of the patent in connection with an investigation of the patent's potential infringement by a third party and in anticipation of litigation.

10. Newly presented claims 86-92 overcome the defects of claims 2-39 and 56-74 by claiming the invention in a

way which eliminates the foregoing unnecessary limitations. In particular, new reissue claim 86 is directed to an integrated circuit for implementing a current-mode switching voltage regulator, the integrated circuit including (1) at least an input terminal, a ground terminal, an output terminal, a feedback terminal and a compensation terminal as specifically recited for connection to external components; (2) a power switching transistor structure coupled to conduct a current between the output terminal and the ground terminal; (3) a circuit coupled to the power switching transistor structure for varying the on and off duty cycle of the switching transistor in response to a control signal; (4) a circuit including a resistive element coupled in series with a current path in the switching transistor structure for generating a current sense signal indicative of the current conducted by the switching transistor; (5) a circuit for generating an error signal indicative of a difference between the feedback signal and a reference signal, and for coupling the error signal to the compensation terminal; (6) a circuit for comparing the current sense signal to the error signal and for generating the control signal to turn off the switching transistor when the current sense signal compares in a predetermined manner to the error signal to vary the duty cycle of the switching transistor to produce the regulated output voltage, the comparing circuit further being responsive to control signal externally applied to the compensation terminal for performing at least one of (a) limiting peak current conducted by the switching transistor, and (b) variably limiting current conducted by the switching transistor as a function of time; and (7) a circuit responsive to a control signal externally applied to a shutdown terminal of the integrated circuit for placing the integrated circuit into a shutdown state where the current drawn by the integrated

circuit is reduced.

11. Newly presented reissue claim 87, dependent from claim 86, more particularly states that the shutdown terminal is the compensation terminal.

12. Newly presented reissue claim 88, which also depends from claim 86, adds that the switching transistor structure is a bipolar transistor.

13. Independent reissue claim 89 is added to recite the elements of the current-mode architecture of my invention without reciting the additional shutdown circuitry. New reissue claim 90, dependent from claim 89, adds a circuit, responsive to a control signal externally applied to a shutdown terminal of the integrated circuit, for reducing the current drawn by the integrated circuit to place the integrated circuit into a shutdown state. New dependent claims 91 and 92, like claims 87 and 88, add respectively that the shutdown terminal is the compensation terminal, and that the switching transistor structure is a bipolar transistor.

14. My invention, as claimed by new reissue claims 86-92, is fully disclosed in and supported by the specification of the '070 patent, as can be seen from my demonstration of support for reissue claims 82-83 in ¶ 11 of my April 5, 1991 declaration.

15. An additional specific error in the '070 patent is the recitation in the claims of the patent that the control signals used to turn off the switching transistor is generated when the current sense signal exceeds the error signal.

16. In the specification of the '070 patent, I described an exemplary integrated circuit embodiment of the invention which includes a comparator circuit 116 (see, e.g., FIG. 1). Comparator 116 receives and compares input signals from amplifiers 114 and 118. Amplifier 114 provides a voltage

signal that is proportional to switch current. Amplifier 118 provides a second voltage signal indicative of the difference between a feedback signal applied to terminal FB and a reference voltage provided by reference voltage generator 120. Comparator 116 operates such that, "during normal feedback operation, switch 110 is turned off when switch current reaches a predetermined level set by the output of error amplifier 118" (col. 6, lines 48-50).

17. In the particular embodiments described in the specification, comparator 116 causes switch 110 to be turned off when the positive magnitude of the voltage signal from current switch amplifier 114 substantially equals or exceeds a threshold level equal to the positive magnitude of the voltage signal from error amplifier 118. It was an error in the claims to recite only that the switch is turned off when a current sense signal exceeds an error signal. There are many ways that a person of ordinary skill in the art could implement, and would understand from the '070 patent how to implement, the comparator function of the present invention. For example, it would be within the scope of the invention to provide a comparator that caused switch 110 to turn off only when the voltage signal from amplifier 114 substantially equals or exceeds a threshold voltage which is a diode drop above, or a diode drop below, the voltage signal from amplifier 118. Also, negative signal voltages could be used. In such circuits, the comparator would still perform the function of comparing the switch current to a predetermined level set by the output of error amplifier 118 to control the duty cycle of the switch.

18. During preparation and prosecution of the applications for the '070 patent, I did not fully appreciate that the claims were limited as set forth in ¶ 15 above. The added reissue claims define the function of the comparator

without reciting the specific predetermined manner in which the comparison between the switch current signal and the output voltage error signal is made, since such a recitation is not necessary to define the metes and bounds of the invention with particularity. It is clear from the claims that the predetermined manner chosen must result in the generation of a control signal that varies the duty cycle of the switching transistor as necessary to regulate output voltage.

19. I hereby acknowledge my duty to disclose to the Patent and Trademark Office information of which I am aware that is material to the examination of this reissue application in accordance with Rule 56 of the Patent Office Rules (37 C.F.R. §1.56(a)).

20. I hereby declare that I understand the English language, and that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements are made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of this application or any patent issued thereon.

21. Applicant hereby appoint CHARLES B. SMITH, Reg. No. 16,763, and MARK D. ROWLAND, Reg. No. 32,077, both of Fish & Neave, 875 Third Avenue, New York, New York 10022-6250, telephone (212) 715-0600, as their principal attorneys of record in connection with the captioned patent, with full power to prosecute this application for reissue and to transact all business in the Patent and Trademark Office in connection

therewith. All correspondence should be sent to Mark D. Rowland at the above address.

Executed March 7, 1994

√ Carl T. Nelson

Carl T. Nelson